Performance And Low Power Driven VLSI Standard Cell Placement Usingtabu Search

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Summary

We engineer a well-known optimization technique namely tabu search (TS) (Sait and Youssef, 1999) for the performance and low power driven VLSI standard cell placement problem (Sait and Youssef, 1995; Minhas, 2001). The above problem is of multiobjective nature since three possibly conflicting objectives are considered to be optimized subject to the constraint of layout width. These objectives are power dissipation, timing performance, and interconnect wire length. It is well known that optimizing cell placement for even a single objective namely total wire length is a hard problem to solve. Due to the imprecise nature of objective values, fuzzy logic is incorporated in the design of the aggregating function. The above technique is applied to the placement of ISCAS-89 benchmark circuits and the results are compared with the Adaptive-bias Simulated Evolution (SimE) approach reported in (Youssef et al., 2001). The comparison shows a significant improvement over the SimE approach